IN THE CLAIMS:

Please amend the claims as follows:

1. (Cancelled)

2. (Currently amended) An input circuit comprising:

delay means for defining a delay time for at least one logical state of a data signal and thereby delaying a clock signal for the delay time defined; and

a holding circuit for holding the data signal responsive to the delayed clock signal;

wherein the delay means comprises:

a comparator for comparing an edge of the clock signal, on which the data signal is intended to be latched, to ~~at least~~ one of a leading edge and a trailing ~~edges~~ edge of the data signal; and

a delay circuit for defining the delay time based on a result of comparison performed by the comparator, and

wherein the delay means defines the delay time such that an edge of the clock signal, on which the data signal is intended to be latched and which is included within a transition interval of the data signal, is delayed to a point in time after the transition interval of the data signal is over.

3. (Currently amended) An input circuit comprising:

delay means for defining a delay time for at least one logical state of a data signal and thereby delaying a clock signal for the delay time defined; and

a holding circuit for holding the data signal responsive to the delayed clock signal;

wherein the delay means comprises:

a comparator for comparing ~~the~~ an edge of the clock signal, which has not been subject to a delay, and on which the data signal is intended to be latched, to ~~at least~~ one of a leading edge and a trailing ~~edges~~ edge of the data signal during each cycle of said clock signal; and

a delay circuit for defining the delay time based on a result of comparison performed by the comparator.

4. (Currently amended) An input circuit comprising:

delay means for defining a delay time for at least one logical state of a data signal and thereby delaying a clock signal for the delay time defined; and

a holding circuit for holding the data signal responsive to the delayed clock signal;

wherein the delay means comprises:

a comparator for comparing an ~~the~~ edge of the clock signal, on which the data signal is intended to be latched, to one of the leading and trailing edges of the data signal;

a first delay circuit for defining the delay time for a logically high state of the data signal based on a result of comparison, performed by the comparator, between one of the leading edges of the data signal and the edge of the clock signal;

a second delay circuit for defining the delay time for a logically low state of the data signal based on a result of comparison, performed by the comparator, between one of the trailing edges of the data signal and the edge of the clock signal; and

a selector for selecting the delay time defined by the first delay circuit when the data signal is in the logically high state or the delay time defined by the second delay circuit when the data signal is in the logically low state.

5. (Previously presented) The input circuit of Claim 3, wherein the delay circuit defines the delay time based on the result of comparison performed by the comparator and a setup time for correctly latching the data signal.

6. (Cancelled)

7. (Cancelled)

8. (Previously presented) The input circuit of Claim 4, wherein the delay means defines the delay time such that an edge of the clock signal, on which the data signal is intended to be latched and which is included within a transition interval of the data signal, is delayed to a point in time after the transition interval of the data signal is over.

9. (Previously presented) The input circuit of claim 4, wherein the first delay circuit defines the delay time based on the result of comparison performed by the comparator, between one of the leading edges of the data signal and the edge of the clock signal, and a setup time for correctly latching the data signal, and the second delay circuit defines the delay time based on the result of comparison performed by the comparator, between one of the trailing edges of the data signal and the edge of the

clock signal, and the setup time for correctly latching the data signal.

10. (Previously presented) The input circuit of claim 3, wherein said edge of the clock signal on which the data signal is intended to be latched is provided to said comparator without being subject to a delay.